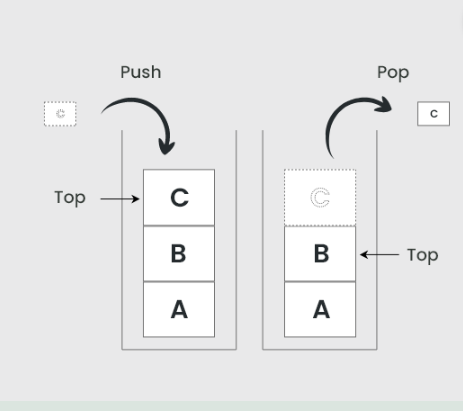
**Frontend design of 16x8 Stack Memory using Synopsys Tools**

**Introduction**

A **Stack** is a linear data structure that follows a particular order in which the operations are performed. The order may be **LIFO (Last In First Out)** or **FILO (First In Last Out)**. **LIFO** implies that the element that is inserted last, comes out first and **FILO** means that the element that is inserted first, comes out last.



**The operations that are used:**

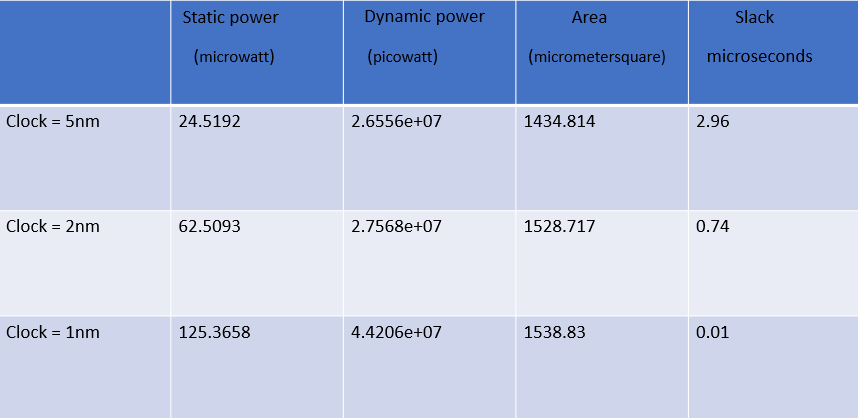
* **Push**: Adds an element to the top of the stack.
* **Pop**: Removes the top element from the stack.
* **Peek**: Returns the top element without removing it.
* **Is Empty**: Checks if the stack is empty.
* **Is Full**: Checks if the stack is full (in case of fixed-size arrays).

**Design and Implementation**

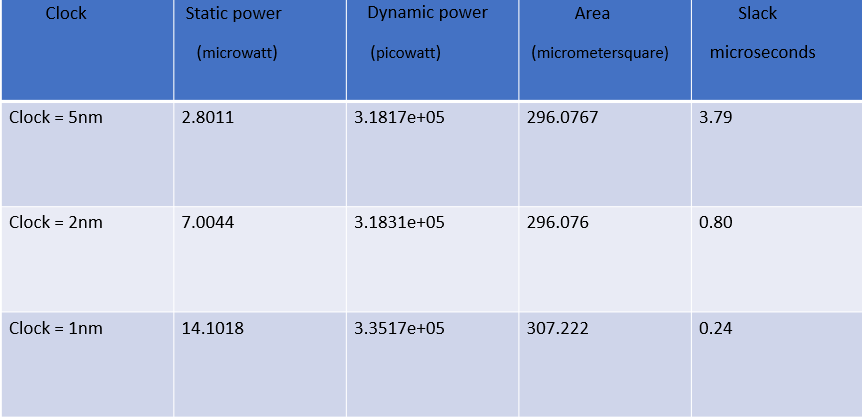
* Specifying the **stack’s behavior** in Verilog.
* Focusing on the critical operations of **push**, and **pop**.
* The Verilog code is written to reflect the **specified behavior.**
* Each operation is **coded**
* Checking **robustness** and **reliability.**

**For synthesis, we used two technologies they are:**

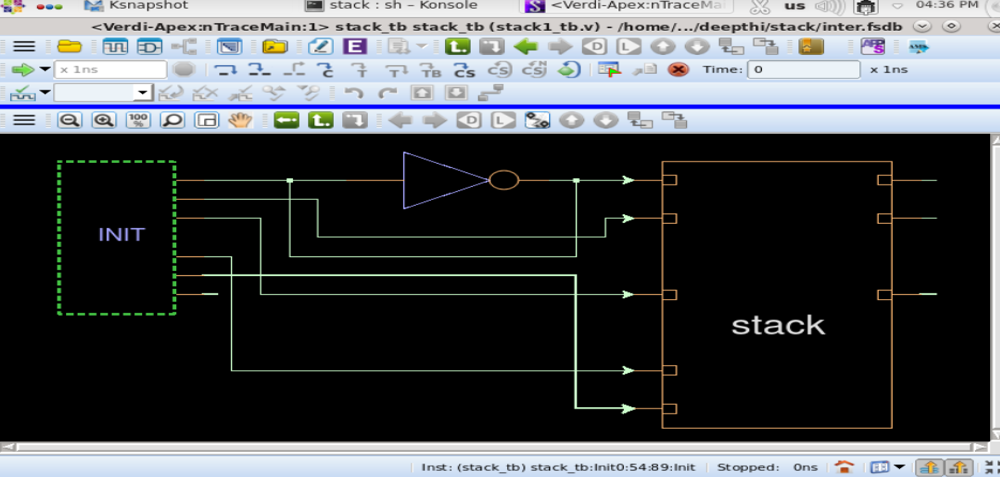
**Synthesis Results Using 28/32 nm Technology**

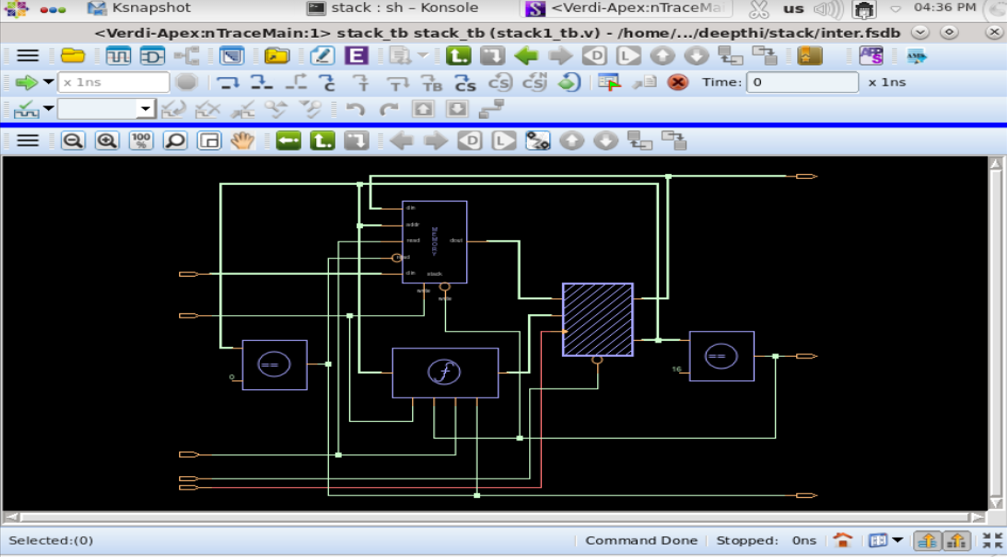


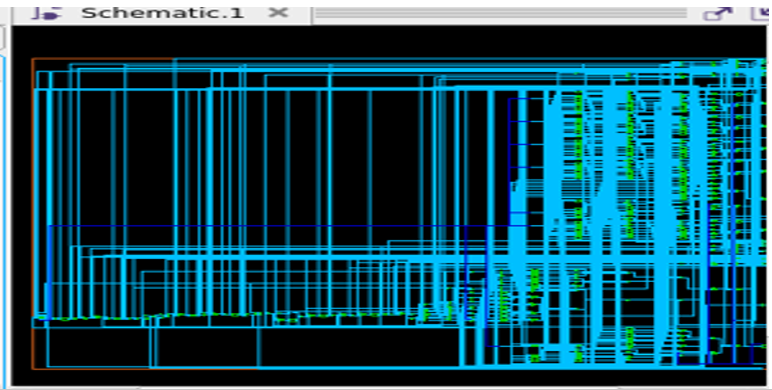
**Synthesis Results Using 14 nm Technology**



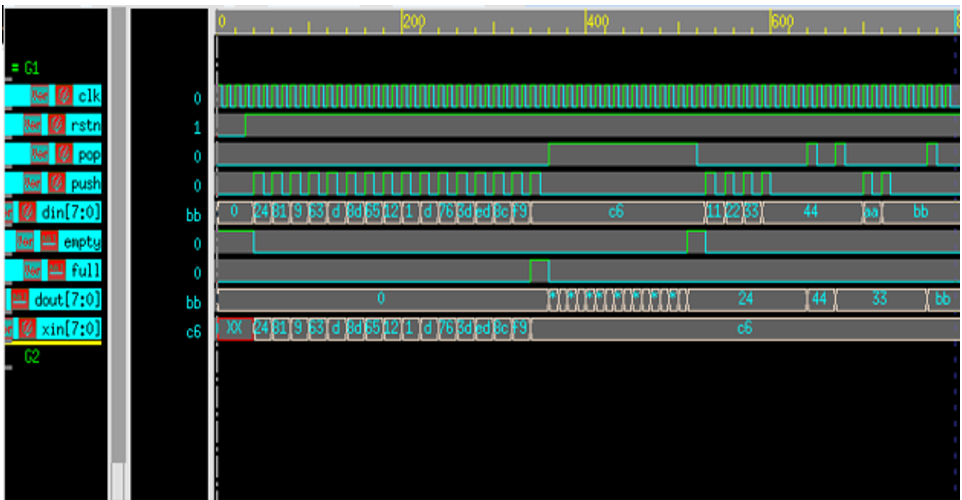
**SCHEMATIC DIAGRAMS**



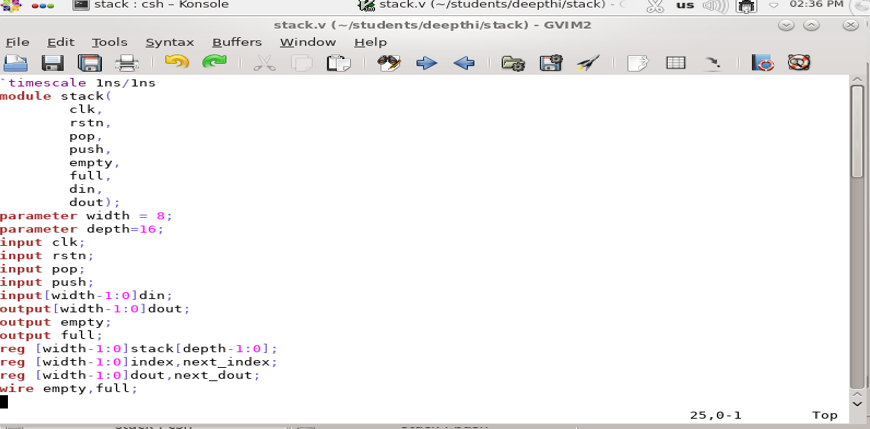


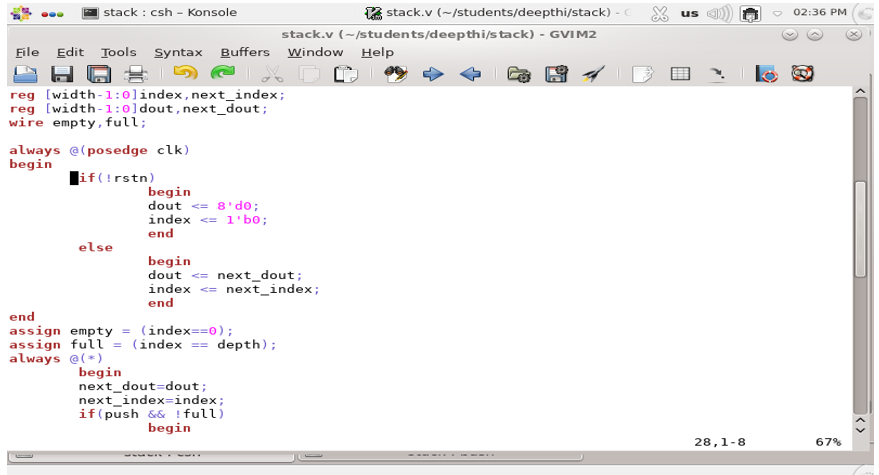


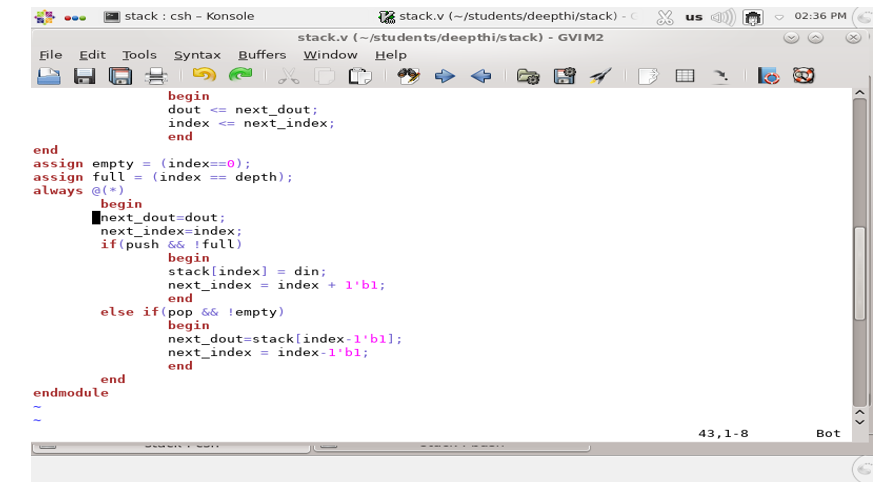
**WAVEFORM**



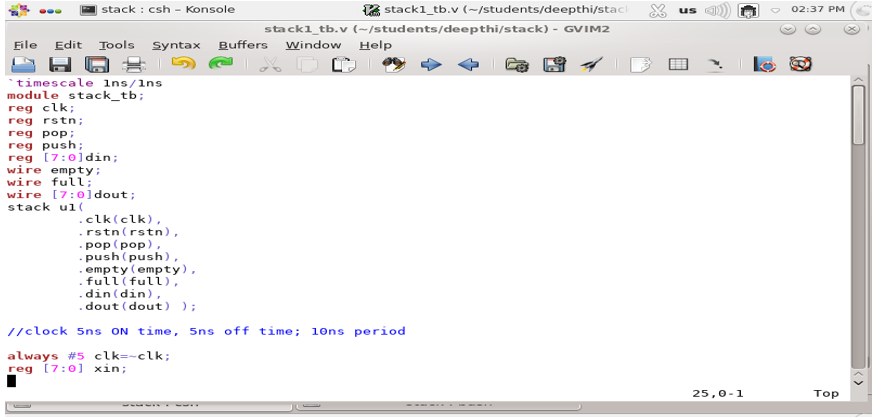
**CODE**

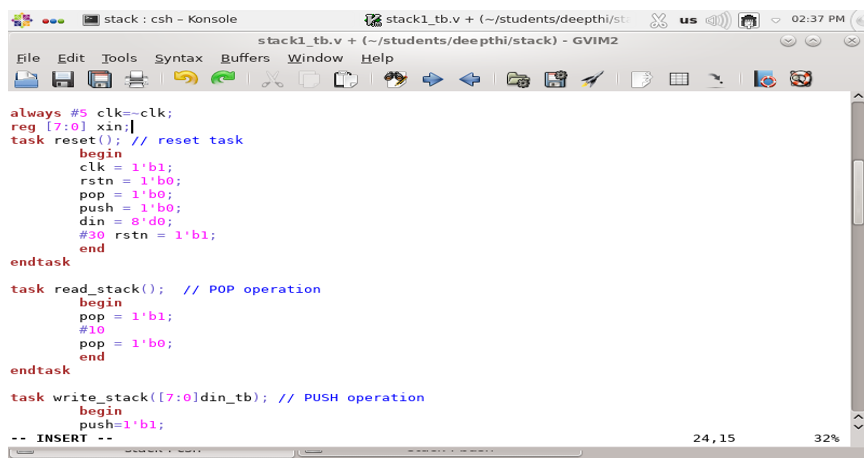


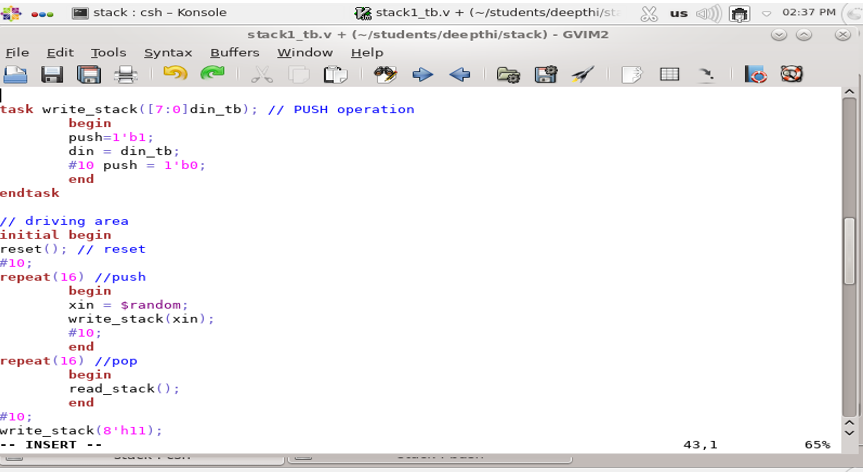


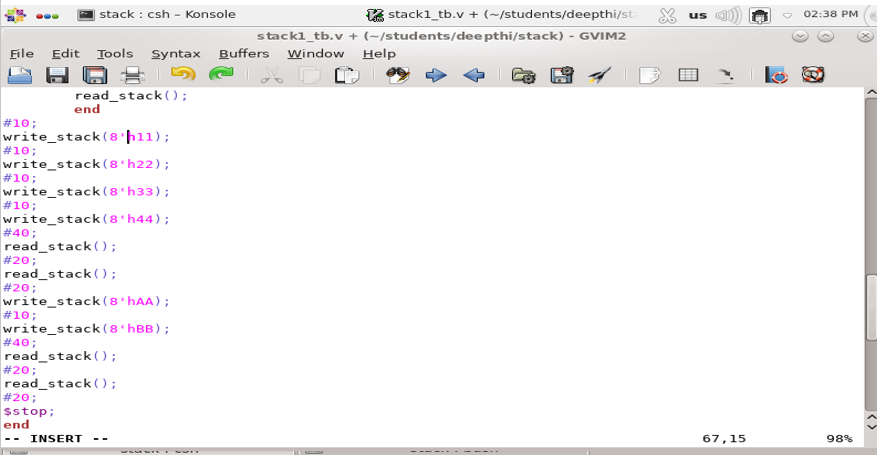


**TESTBENCH**









**Applications of Stack**

1. Converting Infix to Postfix expression
2. Recursion
3. Interrupt handling

**Conclusion**

* This project successfully demonstrates the design, implementation, and verification of a stack memory system using Synopsys VCS, Verdi, and Synthesis.
* The methodologies employed ensure that the stack operates correctly and efficiently, handling various computational tasks as required.
* This approach can be extended to other hardware designs, illustrating the versatility and necessity of EDA tools in modern electronic design verification.

**References**

1. Digital Design and Computer Architecture" by David Harris and Sarah Harris.
2. Synopsys VCS User Guide.
3. Synopsys Verdi User Guide.
4. Synopsys Synthesis User Guide.
5. Research papers on stack memory design, verification, and synthesis.

**This abstract provides a detailed overview of the project's objectives, methodologies, and outcomes, emphasizing the use of advanced EDA tools in ensuring the correctness and performance of stack memory operations.**